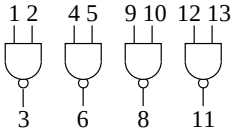
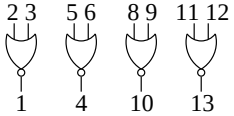
Pinouts for 74LS series for CSC 258

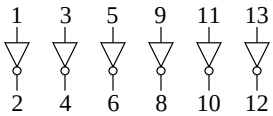
74LS00
four two-input NAND gates



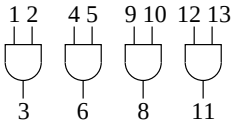
74LS02
four two-input NOR gates



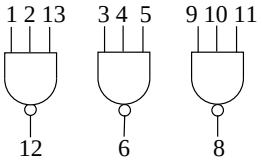
74LS04
six inverters



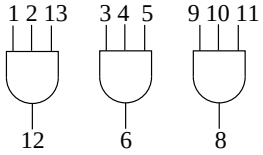
74LS08
four two-input AND gates



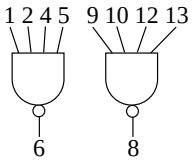
74LS10
three three-input NAND gates



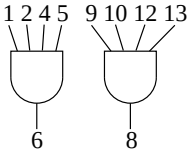
74LS11
three three-input AND gates



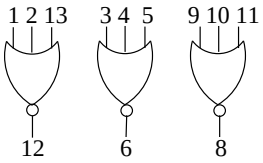
74LS20
two four-input NAND gates



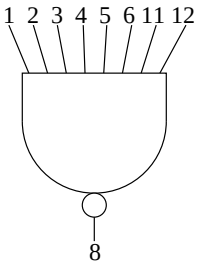
74LS21
two four-input AND gates



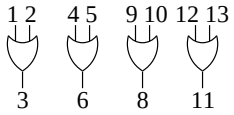
74LS27
three three-input NOR gates



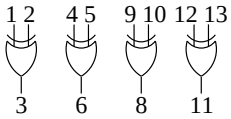
74LS30
one eight-input NAND gate



74LS32
four two-input OR gates



74LS86
four two-input XOR gates



74LS153
two 4-to-1 multiplexers

func	pin	func	pin
$\overline{\text{ENABLE}}$	1	$\overline{\text{ENABLE}}$	15
x_3	3	x_3	13
x_2	4	x_2	12
x_1	5	x_1	11
x_0	6	x_0	10
y	7	y	9

Common select:

s_1	2
s_0	14

74LS253: two tri-state 4-to-1 multiplexers.
As 74LS153 but if ENABLE is 0, output is not driven.

74LS283: four-bit adder:

Inputs:

(a_3,a_2,a_1,a_0) on pins 12, 14, 3, 5
(b_3,b_2,b_1,b_0) on pins 11, 15, 2, 6
carry-in on pin 7

Outputs:

(s_3,s_2,s_1,s_0) (sum) on pins 10, 13, 1, 4
carry-out on pin 9

74LS74
two independent D flip-flops

func	pin	func	pin
D	2	D	12
$\overline{\text{Set}}$	4	$\overline{\text{Set}}$	10
$\overline{\text{Reset}}$	1	$\overline{\text{Reset}}$	13
Clock	3	Clock	11
Q	5	Q	9
$\overline{\text{Q}}$	6	$\overline{\text{Q}}$	8

74LS174
six-bit D flip-flop with reset

func	pin
D_0	3
D_1	4
D_2	6
D_3	11
D_4	13
D_5	14
Clock	9
$\overline{\text{Reset}}$	1
Q_0	2
Q_1	5
Q_2	7
Q_3	10
Q_4	12
Q_5	15

74LS175
four-bit D flip-flop with reset

func	pin
D_0	4
D_1	5
D_2	12
D_3	13
Clock	9
$\overline{\text{Reset}}$	1
Q_0	2
$\overline{Q_0}$	3
Q_1	7
$\overline{Q_1}$	6
Q_2	10
$\overline{Q_2}$	11
Q_3	15
$\overline{Q_3}$	14

74LS195
four-bit parallel-access shift register

func	pin
D_0	4
D_1	5
D_2	6
D_3	7
F1	2
$\overline{\text{F2}}$	3
$\overline{\text{LOAD}}$	9
Clock	10
$\overline{\text{RESET}}$	1
Q_0	15
Q_1	14
Q_2	13
Q_3	12
$\overline{Q_3}$	11

The shift (if $\overline{\text{LOAD}}$) is $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$. F1 and F2 control the inserted bit when shifting.

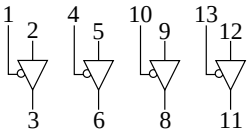
If F1=F2,
$Q_0 \leftarrow$ F1.

Else if F2=1,
$Q_0 \leftarrow Q_0$.

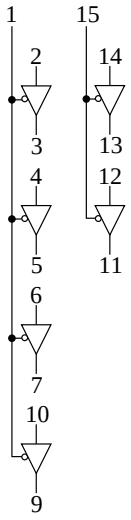
Else $Q_0 \leftarrow \overline{Q_0}$.

The RESET is asynchronous.

74LS125
four tri-state buffers



74LS367A
one four-bit and one two-bit tri-state buffers



Omitted: 74LS191 and 74LS193 (counters)

Also omitted: all open-collector variants

Pinouts for digital I/O board ribbon cable

Lower side	Upper side
1 − switch 1	2 − switch 2
3 − switch 3	4 − switch 4
5 − switch 5	6 − switch 6
7 − switch 7	8 − switch 8
9 − ground	10 − not connected
11 − ground	12 − not connected
13 − ground	14 − not connected
15 − ground	16 − not connected
17 − $\overline{\text{LED 1}}$	18 − $\overline{\text{LED 2}}$
19 − $\overline{\text{LED 3}}$	20 − $\overline{\text{LED 4}}$
21 − $\overline{\text{LED 5}}$	22 − $\overline{\text{LED 6}}$
23 − $\overline{\text{LED 7}}$	24 − $\overline{\text{LED 8}}$
25 − ground	26 − not connected
27 − ground	28 − not connected
29 − ground	30 − not connected
31 − ground	32 − not connected
33 − CLK (output)	34 − not connected
35 − not connected	36 − not connected
37 − not connected	38 − $\overline{\text{pulse switch}}$
39 − not connected	40 − not connected

The switches (including the pulse switch) are outputs from the digital board, and the LEDs are inputs to the digital board.

For CSC 258 labs, we will not be using the clock (pin 33). It provides regular clock pulses for more interesting circuits. In our labs, when we do have a clock we will want to perform the clock pulses by hand so as to be able to see each state of the circuit. So we will use an input switch (or the pulse switch) for the clock line for any circuit in the CSC 258 labs.